

Category: Bulk SMS One of the trends in the semiconductor industry in recent years has been the use of larger circuit structures, such as memory circuit structures, integrated circuit (IC) designs, and the like, and the use of silicon-on-insulator (SOI) substrate designs. As will be understood by those skilled in the art, SOI designs take advantage of the fact that silicon is not a great conductor of electricity and are able to be made with only a thin layer of silicon on top of an insulator, such as silicon dioxide. However, this thin layer of silicon is a very useful layer in that it can be used as a transistor and electrical interconnection layer in a very large scale integrated circuit (VLSI) design. The large scale of the circuits has resulted in the need for very thin gate insulators in order to achieve sufficiently low gate-to-drain capacitance, gate-to-source capacitance, and the like, to enable the circuit to operate properly with this thin gate insulator. In order to create a VLSI circuit design, one must consider how to lay out the silicon, the insulators, the active transistors and the interconnections that will be utilized to create the circuitry. In the past, there were no clear standards or procedures for the designers in this regard. Consequently, the designers tended to design the circuit in what was thought to be a correct manner. These layouts would then be "implemented" in the manufacturing process to create the circuit. For example, an integrated circuit design was created and then laid out on a typical semiconductor wafer. Then, in the manufacturing process, the transistors and interconnections were created on the surface of the substrate. Unfortunately, in this type of process, the layout had to be completely rebuilt in each device in the manufacturing facility. Further, each device being constructed, such as VLSI, typically had to be completely redesigned in the manufacturing facility for each device. Consequently, a VLSI circuit design is typically implemented in a number of different semiconductor wafers which are all assembled into a multichip module (MCM) for packaging into a final product. Furthermore, the final product may be a system on a chip (SOC), system on a module (SOM), or the like. During the manufacturing process, it is normally desirable to create as many of the devices as possible, while not creating too many defects. This is to increase the yield



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